

This diagram shows a cross-section of a semiconductor device. The substrate 1 consists of multiple layers: a bottom layer 5, a middle layer 6, and a top layer 7. A gate stack 8 is positioned above layer 7, comprising a polysilicon gate 4 and a PRG (Polysilicon Residual Gate) layer. An etch stop layer E is situated between layers 6 and 7. A circular feature is indicated by a circle and an arrow pointing to it from the left.